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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,069	10/28/2003	William J. Dally	2789.2003-001	4177

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EXAMINER	
CHOI, EUNSOOK	
ART UNIT	**PAPER NUMBER**
2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/695,069	DALLY ET AL.	
	Examiner	Art Unit	
	Eunsook Choi	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/23/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: Claim 1 has "the higher frequency data multiplexer" and "the lower frequency data multiplexer". Appropriate correction is required.

For a prior art search, the examiner interprets the higher frequency data multiplexer as the higher frequency data demultiplexer and the lower frequency data multiplexer as the lower frequency data demultiplexer".

2. Claim 2 is objected to because of the following informalities: Claim 2 has " the higher frequency data multiplexing stage " and "the lower frequency data multiplexing stage". Appropriate correction is required.

For a prior art search, the examiner interprets the higher frequency data multiplexing stage as a higher frequency data (de)multiplexing stage and the lower frequency data multiplexing stage as a lower frequency data (de)multiplexing stage.

3. Claims 2-11 are objected to as incorporating the deficiencies of a claim upon which it depends. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, Claim 1 recites the limitation "the higher frequency data multiplexer" and "the lower frequency data multiplexer". There is insufficient antecedent basis for this limitation in the claim.

Regarding claim 2, Claim 2 recites the limitation " the higher frequency data multiplexing stage " and "the lower frequency data multiplexing stage". There is insufficient antecedent basis for this limitation in the claim.

Claims 2-11 are rejected to as incorporating the deficiencies of a claim upon which it depends

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1, 5, 6, 8, 9, 10, 12, 16, 17, 19, 20, 12, 21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Izadpannah (US Patent 6240274) in view of Lundh et al. (US Patent 6310895, hereinafter Lundh).

Regarding claim 1, Izadpannah teaches the high bit-rate electrical serial signal (a higher frequency data) is passed to a demultiplexer (a higher frequency data demultiplexer) controlled by a master clock(a clock source), the signal is demultiplexed into N parallel sub-rate digital channels (demultiplexing the higher frequency data on the communication link to an intermediate frequency signal), the resulting channels are then applied to a bank of individual modems (a lower frequency data demultiplexer). Each individual modem of the bank of individual modems is synchronized by a clock signal from a divider which divides (further demultiplexing the intermediate frequency signal to a lower frequency data) the frequency of the master clock by N (Col. 3 Lines 50-62). Izadpannah teaches the multiplexer, 7 in Fig. 1, is coupled to the a bank of individual modems, 11 in Fig. 1. Izadpannah further teaches the precise value of N is selected to facilitate the desired operating bit-rate per channel in view of the carrier frequencies used and the bit-rate of the incoming digital multiplexed signal from the high bit-rate data transfer means (the clock signal distributed to the lower frequency data).

However, Izadpannah does not expressly teach a clock signal from the clock source being precisely distributed to the higher frequency data demultiplexer and the clock signal being less precisely distributed to the lower frequency data demultiplexer. Lundh in the same field of endeavor teaches, for distribution of clocking rates, where the

high frequency clock is distributed separated from the low frequency synch rate, the precision must be great (Col 1, Lines 58-63 Lundh). It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a clock signal being precisely distributed to the higher frequency data demultiplexer and the clock signal being less precisely distributed to the lower frequency data demultiplexer because the pulses in the synch rate will not end up or be interpreted at the wrong one of the edges of the clock rate pulses (Col 1, Lines 58-63 Lundh).

Regarding claim 12, Izadpannah teaches the high bit-rate electrical serial signal is passed to a demultiplexer controlled by a master clock, the signal is demultiplexed into N parallel sub-rate digital channels (demultiplexing the data from the communication link to an intermediate frequency signal), the resulting channels are then applied to a bank of individual modems. Each individual modem of the bank of individual modems is synchronized by a clock signal from a divider which divides (further demultiplexing the intermediate frequency signal to a lower frequency signal) the frequency of the master clock by N (Col. 3 Lines 50-62).

However, Izadpannah does not expressly teach using a clock signal precisely distributed from a clock source and using the clock signal less precisely distributed from the clock source. Lundh in the same field of endeavor teaches, for distribution of clocking rates, where the high frequency clock is distributed separated from the low frequency synch rate, the precision must be great (Col 1, Lines 58-63 Lundh). It would have been obvious to one having ordinary skill in the art at the time the invention was

made to use a clock signal precisely distributed from a clock source and to use the clock signal less precisely distributed from the clock source because the pulses in the synch rate will not end up or be interpreted at the wrong one of the edges of the clock rate pulses (Col 1, Lines 58-63 Lundh).

Regarding claim 23, Izadpannah teaches the high bit-rate electrical serial signal is passed to a demultiplexer controlled by a master clock, the signal is demultiplexed into N parallel sub-rate digital channels (high frequency data multiplexer means relying on a clock signal precisely distributed from a clock source for demultiplexing the data on the communication link to an intermediate frequency signal), the resulting channels are then applied to a bank of individual modems. Each individual modem of the bank of individual modems is synchronized by a clock signal from a divider which divides (lower frequency data demultiplexer for demultiplexing the intermediate frequency signal) the frequency of the master clock by N (Col. 3 Lines 50-62). However, Izadpannah does not expressly teach relying on a clock signal precisely distributed from a clock source and relying on the clock signal less precisely distributed from the clock source. Lundh in the same field of endeavor teaches, for distribution of clocking rates, where the high frequency clock is distributed separated from the low frequency synch rate, the precision must be great (Col 1, Lines 58-63 Lundh). It would have been obvious to one having ordinary skill in the art at the time the invention was made to rely on a clock signal precisely distributed from a clock source and to rely on the clock signal less precisely distributed from the clock source because the pulses in the synch rate will not

end up or be interpreted at the wrong one of the edges of the clock rate pulses (Col 1, Lines 58-63 Lundh).

Regarding claims 5 and 16, Izadpannah and Lundh teach all the limitations of claims 1 and 12. Izadpannah teaches each individual modem of the bank of individual modems is synchronized by a clock signal from a divider which divides the frequency of the master clock by N (Col 3, Lines 57-60, Izadpannah).

Regarding claims 6 and 17, Izadpannah and Lundh teach all the limitations of claims 5 and 16. Izadpannah teaches utilizing methods such as quadrature phase shift keying (QPSK) or quadrature amplitude modulation (QAM) on radio frequency (RF) carriers (frequency divided by a ring counter). Izadpannah further teaches each individual modem of the bank of individual modems is synchronized by a clock signal from the divider which the frequency of the master clock by N. The frequency of the master RF local oscillator is N times multiplied by the harmonic generator to generate a series of N equally spaced carrier frequencies to be applied to the modems. (Col 4, Lines 31-35, Izadpannah).

Regarding claims 8 and 19, Izadpannah and Lundh teach all the limitations of claims 1 and 12. Izadpannah teaches a high bit-rate serial data transmission (one-bit-wide bitstream) from a high bit-rate data transfer means, such as a broadband fiber

optic cable, a signal from a synchronous optical network or a signal in asynchronous transfer mode format (Col 3, Lines 34-50, Izadpannah).

Regarding claims 9 and 20, Izadpannah and Lundh teach all the limitations of claims 8 and 19. Izadpannah teaches the signal is demultiplexed into N parallel (two bits wide) sub-rate digital channels(intermediate frequency signal) where N is a constant integer (Col 3, Lines 52-53 and Line 66, Izadpannah).

Regarding claims 10 and 21, Izadpannah and Lundh teach all the limitations of claims 1 and 20. Izadpannah teaches the signal is demultiplexed into N parallel (more than two parallel bits) sub-rate digital channels(intermediate frequency signal) (Col 3, Lines 52-53, Izadpannah).

9. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Izadpannah (US Patent 6240274) in view of Kishigami et al. (US Patent 5787132, hereinafter Kishigami)

Regarding claim 24, Izadpannah teaches the high bit-rate electrical serial signal is passed to a demultiplexer controlled by a master clock, the signal is demultiplexed into N parallel sub-rate digital channels (demultiplexing data from a communication link comprising: a higher frequency data demultiplexer), the resulting channels are then applied to a bank of individual modems (a lower frequency data demultiplexer). Each

individual modem of the bank of individual modems is synchronized by a clock signal from a divider which divides (further demultiplexes the intermediate frequency signal) the frequency of the master clock by N (Col. 3 Lines 50-62). Izadpannah teaches the multiplexer, 7 in Fig. 1, is coupled to the a bank of individual modems, 11 in Fig. 1.

However, Izadpannah does not expressly teach an electronic chip for a higher frequency data demultiplexer and a lower frequency data demultiplexer. Kishigami, in the same field of endeavor, teaches the clock generating circuit can be formed on one chip together with other components (Col. 7 Lines 15-21, Kishigami). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a higher frequency data demultiplexer and a lower frequency data demultiplexer on an electronic chip to simplify the structure of the unit further and to implement the unit inexpensively (Col. 7 Lines 15-21, Kishigami).

10. Claims 2, 3, 4, 13, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Izadpannah (US Patent 6240274) in view of Lundh et al. (US Patent 6310895, hereinafter Lundh) and in further view of Kishigami et al. (US Patent 5787132).

Regarding claims 2 and 13, Izadpannah and Lundh teach all the limitations of claims 1 and 12. However, Izadpannah and Lundh do not expressly teach a higher frequency data multiplexing stage and a lower frequency data multiplexing stage are formed on a single circuit chip. Kishigami, in the same field of endeavor, teaches the

clock generating circuit can be formed on one chip together with other components (Col. 7 Lines 15-21, Kishigami). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form higher frequency data multiplexing stage and a lower frequency data multiplexing stage on a single circuit chip to simplify the structure of the unit further and to implement the unit inexpensively (Col. 7 Lines 15-21, Kishigami).

Regarding claims 3 and 14, Izadpannah, Lundh and Kishigami teach all the limitations of claims 2 and 13. Izadpannah teaches each individual modem of the bank of individual modems is synchronized by a clock signal from a divider which divides the frequency of the master clock by N (Col 3, Lines 57-60, Izadpannah).

11. Claims 4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Izadpannah (US Patent 6240274) in view of Lundh et al. (US Patent 6310895, hereinafter) and Kishigami et al. (US Patent 5787132) in further view of Ishikawa (US Patent 6310913, hereinafter Ishikawa).

Regarding claims 4 and 15, Izadpannah, Lundh and Kishigami teach all the limitations of claims 3 and 14. However, Izadpannah, Lundh and Kishigami do not expressly teach frequency divided by a ring counter. Ishikawa teaches the ring counter counts clock pulses in cycles to generate and output serially a right-angled triangular sawtooth pulse signal having a certain relationship with the cycle of a reference signal. (Col 6, Lines 25-33, Ishikawa). It would have been obvious to one having ordinary skill

in the art at the time the invention was made to have clock signal with frequency divided by a ring counter to have no phase change and a high resolution and gradually increase the carrier frequency arbitrarily at the low pulsating component (Col 2, Lines 56-59, Ishikawa).

12. Claims 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Izadpannah (US Patent 6240274) in view of Lundh et al. (US Patent 6310895) and in further view of Chang (US Patent 6628605, hereinafter Chang).

Regarding claims 7 and 18, Izadpannah and Lundh teach all the limitations of claims 1 and 12. However, Izadpannah and Lundh do not expressly teach clocked by a multiplying delay locked loop bit clock generator. Chang, in the same field of endeavor, teach the use of a delay locked loop circuit (Col. 2 line 63 – Col 3 Line 4, Chang). It would have been obvious to one having ordinary skill in the art at the time the invention was made to clock by a multiplying delay locked loop bit clock generator in generating clock signal to reduce jitter involve transmitting each data signal (Col. 2 line 63 – Col 3 Line 4, Chang).

13. Claims 11 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Izadpannah (US Patent 6240274) in view of Lundh et al. (US Patent 6310895) and in further view of Fiedler (US Patent 5724361, hereinafter Fiedler).

Regarding claims 11 and 22, Izadpannah and Lundh teach all the limitations of claims 10 and 21. However, Izadpannah and Lundh do not expressly teach clocked by an N-phase overlapping clock. Fiedler, in the same field of endeavor, teaches a high performance n:1 multiplexer and a multiplexer having control over the overlap of multiphase clocks (Col 1 line 6-8 Fiedler). It would have been obvious to one having ordinary skill in the art at the time the invention was made to clock by an N-phase overlapping clock because the characteristics of the clock signal are a critical design concern for multiplexers that are used in high speed digital systems and clock frequency is one factor which determines the rate of data transmission (Col 1, line 19-22 Fiedler).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

a. Yanagimachi (US Patent 3932698, Multiplex signal transmission system) disloses multiplexers 27 and 45 in Fig. 2.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eunsook Choi whose telephone number is 571-270-1822. The examiner can normally be reached on Monday-Friday 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eunsook Choi
6/28/2007

CHARLES D. GARBER
SUPERVISORY PATENT EXAMINER